intel®

8022
SINGLE COMPONENT 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

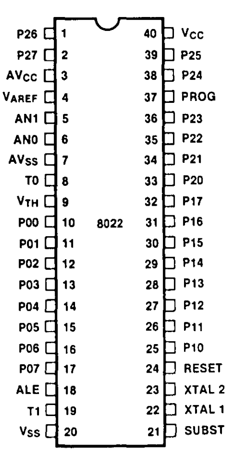
- 8-Bit CPU, ROM, RAM, I/O in Single 40-Pin Package
- On-Chip 8-Bit A/D Converter; Two Input Channels
- 8 Comparator Inputs (Port 0)
- Zero-Cross Detection Capability
- Single 5V Supply (4.5V to 6.5V)
- High Current Drive Capability — 2 Pins
- Two Interrupts — External and Timer
- 2K × 8 ROM, 64 × 8 RAM, 28 I/O Lines
- 10 μsec Cycle; All Instructions 1 or 2 Cycles
- Instructions — 8048 Subset
- Interval Timer/Event Counter
- Clock Generated with Single Resistor, Inductor, or Crystal
- Easily Expandable I/O

The Intel® 8022 is the newest member of the MCS-48™ family of single chip 8-bit microcomputers. It is designed to satisfy the requirements of low cost, high volume applications which involve analog signals, capacitive touchpanel keyboards, and/or large ROM space. The 8022 addresses these applications by integrating many new functions on-chip, such as A/D conversion, comparator inputs and zero-cross detection.

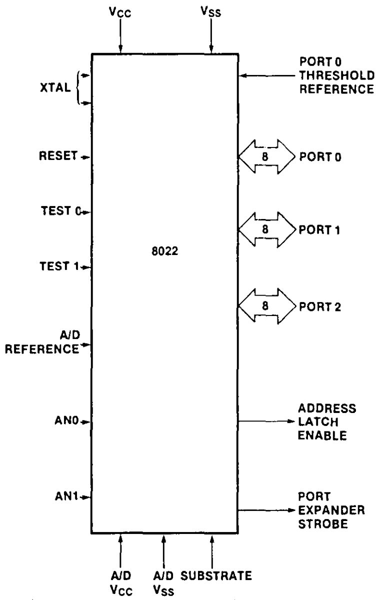
The features of the 8022 include 2K bytes of program memory (ROM), 64 bytes of data memory (RAM), 28 I/O lines, an on-chip 8-bit A/D converter with two input channels, an 8-bit port with comparator inputs for interfacing to low voltage capacitive touchpanels or other non-TTL interfaces, external and timer interrupts, and zero-cross detection capability. In addition, it contains the 8-bit interval timer/event counter, on-board oscillator and clock circuitry, single 5V power supply requirement, and easily expandable I/O structure common to all members of the MCS-48 family.

The 8022 is designed to be an efficient controller as well as an arithmetic processor. It has bit handling capability plus facilities for both binary and BCD arithmetic. Efficient use of program memory results from using the MCS-48 instruction set which consists mostly of single byte instructions and has extensive conditional jump and direct table lookup capability. Program memory usage is further reduced via the 8022's hardware implementation of the A/D converter which simplifies interfacing to analog signals.

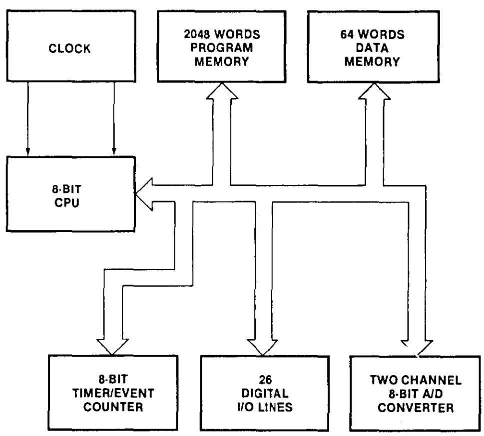
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN DESCRIPTION

Designation	Pin #	Function
V_{SS}	20	Circuit GND potential.
V_{CC}	40	+5V circuit power supply.
PROG	37	Output strobe for Intel® 8243 I/O expander.
P00-P07 Port 0	10-17	8-bit open-drain port with comparator inputs. The switching threshold is set externally by V_{TH}. Optional pull-up resistors may be added via ROM mask selection.
V_{TH}	9	Port 0 threshold reference pin.
P10-P17 Port 1	25-32	8-bit quasi-bidirectional port.
P20-P27	33-36	8-bit quasi-bidirectional port.
Port 2	38-39 1-2	P20-23 also serve as a 4-bit I/O expander for Intel® 8243.
T0	8	Interrupt input and input pin testable using the conditional transfer instructions JT0 and JNT0. Initiates an interrupt following a low level input if interrupt is enabled. Interrupt is disabled after a reset.
T1	19	Input pin testable using the JT1 and JNT1 conditional transfer instructions. Can be designated the timer/event counter input using the STRT CNT instruction. Also serves as the zero-cross detection input to allow zero-crossover sensing of slowly moving AC inputs. Optional pull-up resistor may be added via ROM mask selection.

Designation	Pin #	Function
RESET	24	Input used to initialize the processor by clearing status flip-flops and setting the program counter to zero.
AV_{SS}	7	A/D converter GND Potential. Also establishes the lower limit of the conversion range.
AV_{CC}	3	A/D +5V power supply.
SUBST	21	Substrate pin used with a bypass capacitor to stabilize the substrate voltage and improve A/D accuracy.
V_{AREF}	4	A/D converter reference voltage. Establishes the upper limit of the conversion range.
AN0, AN1	6,5	Analog inputs to A/D converter. Software selectable on-chip via SEL AN0 and SEL AN1 instructions.
ALE	18	Address Latch Enable. Signal occurring once every 30 input clocks (once every single cycle instruction), used as an output clock.
XTAL 1	22	One side of crystal, inductor, or resistor input for internal oscillator. Also input for external frequency source. (Not TTL compatible.)
XTAL 2	23	Other side of timing control element. This pin is not connected when an external frequency source is used.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ....0°C to 70°C
Storage Temperature ....-65°C to +180°C
Voltage on Any Pin with
Respect to Ground ....-0.5V to +7V
Power Dissipation ....1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permenent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage (All except XTAL 1, XTAL 2, Port 0)	-0.5		0.8	V	
V_{IL1}	Input Low Voltage (Port 0)	-0.5		$V_{TH} - 0.1$	V	
V_{IH}	Input High Voltage (All except XTAL 1, XTAL 2, RESET, Port 0)	2.0		V_{CC}	V	$V_{CC} = 5.0V \pm 10\%$
V_{IH1}	Input High Voltage (All except XTAL 1, XTAL 2, RESET, Port 0)	2.4		V_{CC}	V	$V_{CC} = 6.0V \pm 0.5V$
V_{IH2}	Input High Voltage (Port 0)	$V_{TH} + 0.1$		V_{CC}	V	
V_{IH3}	Input High Voltage (RESET, XTAL 1)	3.0		V_{CC}	V	
V_{TH}	Port 0 Threshold Reference Voltage	0		$V_{CC}/2$	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{IL} = 1.6$ mA
V_{OL1}	Output Low Voltage (P10, P11)			2.5	V	$I_{OL} = 7$ mA
V_{OH}	Output High Voltage (All unless Open Drain Option—Port 0)	2.4			V	$I_{OH} = 50\ \mu A$
I_{LI}	Input Leakage Current (T1)			±10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage Current (Open Drain Option—Port 0)			±10	μA	$V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$
I_{CC}	V_{CC} Supply Current			80	mA	
V_{T1}	Zero-Cross Detection Input (T1)	1		3	VACpp	Input through a capacitor

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Cycle Time	10.0	50.0	μs	3 MHz XTAL = 10 μs
t_{LL}	ALE Pulse Width	4.6		μs	$t_{CY} = 10\ \mu s$
Δ_F	Oscillator Frequency Variation—Resistor Mode	-20	+20	%	F = 2.5 MHz, R = 15 kΩ
F_{T1}	Zero-Cross Detection Input Frequency (T1)	0.03	1	kHz	

A.C. TEST CONDITIONS

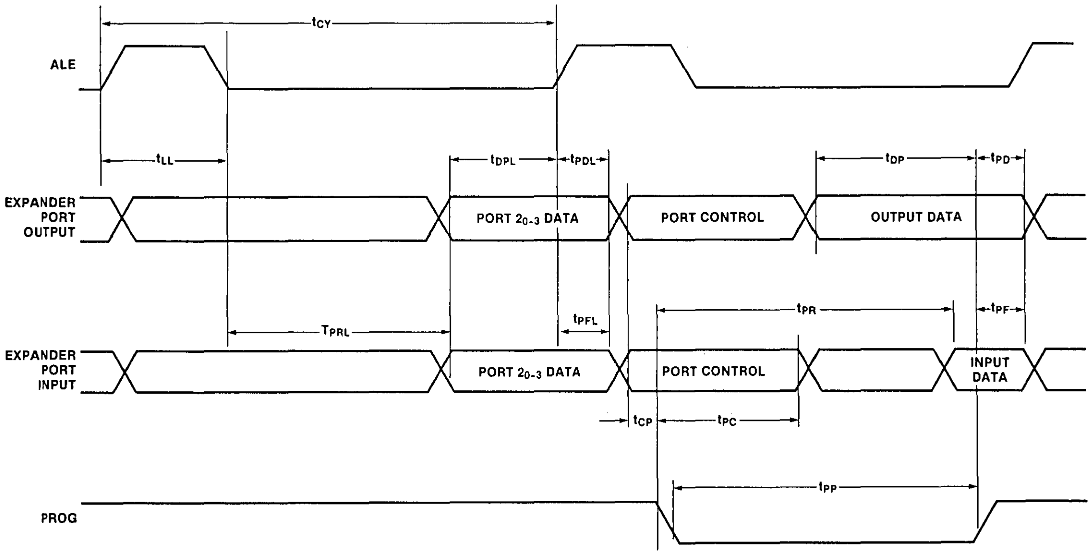
Control Outputs: $C_L = 80$ pF

A.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$

	Symbol	Parameter	Min.	Max.	Unit	Notes
Expander Operation	t_{CP}	Port Control Setup Before Falling Edge of PROG	110		ns	
	t_{PC}	Port Control Hold After Falling Edge of PROG	140		ns	
	t_{PR}	PROG to Time P2 Input Must Be Valid		810	ns	
	t_{DP}	Output Data Setup Time	220		ns	
	t_{PD}	Output Data Hold Time	65		ns	
	t_{PF}	Input Data Hold Time	0	150	ns	
	t_{PP}	PROG Pulse Width	1510		ns	
Normal Operation	t_{PRL}	ALE to Time P2 Input Must Be Valid	810		ns	
	t_{DPL}	Output Data Setup Time	400		ns	
	t_{PDL}	Output Data Hold Time	150		ns	
	t_{PFL}	Input Data Hold Time	110		ns	

PORT 2 TIMING

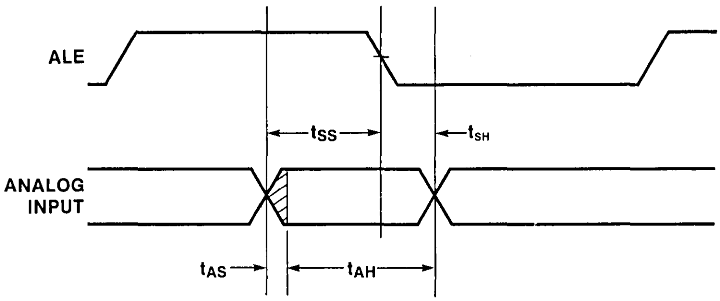


A/D CONVERTER CHARACTERISTICS

$T_A = 0°C$ to $70°C$, $V_{CC} = 5.5V \pm 1V$, $V_{SS} = 0V$, $AV_{CC} = 5.5V \pm 1V$, $AV_{SS} = 0V$

Parameter	Min.	Typ.	Max.	Unit	Comments
Resolution	8			Bits	
Non-Linearity		± ½		LSB	(Note 1)
Zero Error		0		LSB	(Note 2) $T_A = 25°C$
Full Scale Error		0		LSB	(Note 3) $T_A = 25°C$
Quantization Error		± ½		LSB	(Note 4)
Absolute Accuracy		± 1		%	(Note 5)
Conversion Range	AV_{SS}		V_{AREF}	V	
V_{AREF}	$AV_{CC}/2$		AV_{CC}	V	
Input Capacitance (AN0, AN1)		1		pF	
Conversion Time	4		4	t_{CY}	
Sample Hold Time (t_{AS})		0.07		t_{CY}	(Note 6)
Sample Hold Time (t_{AH})		0.23		t_{CY}	(Note 6)
Sample Setup Before Falling Edge of ALE (t_{SS})		0.20		t_{CY}	
Sample Hold After Falling Edge of ALE (t_{SH})		0.10		t_{CY}	

ANALOG INPUT TIMING



NOTES:

1. Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristics.
2. Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage.
3. Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage.
4. Quantization error is the uncertainty caused by the converters finite resolution.
5. Absolute accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output. Included are quantizing and all other errors.
6. The analog input must be maintained at a constant voltage during the sampling time (t_{AS}) and the sample hold time (t_{AH}).

INSTRUCTION SET

	Mnemonic	Description	Bytes	Cycle	Hexadecimal Opcode
Accumulator	ADD A,R_r	Add register to A	1	1	68-6F
	ADD A,@R	Add data memory to A	1	1	60-61
	ADD A,#data	Add immediate to A	2	2	03
	ADDC A,R_r	Add register with carry	1	1	78-7F
	ADDC A,@R	Add data memory with carry	1	1	70-71
	ADDC A,#data	Add immediate with carry	2	2	13
	ANL A,R_r	And register to A	1	1	58-5F
	ANL A,@R	And data memory to A	1	1	50-51
	ANL A,#data	And immediate to A	2	2	53
	ORL A,R_r	Or register to A	1	1	48-4F
	ORL A,@R	Or data memory to A	1	1	40-41
	ORL A,#data	Or immediate to A	2	2	43
	XRL A,R_r	Exclusive Or register to A	1	1	D8-DF
	XRL A,@R	Exclusive Or data memory to A	1	1	D0-D1
	XRL A,#data	Exclusive Or immediate to A	2	2	D3
	INC A	Increment A	1	1	17
	DEC A	Decrement A	1	1	07
	CLR A	Clear A	1	1	27
	CPL A	Complement A	1	1	37
	DA A	Decimal adjust A	1	1	57
	SWAP A	Swap nibbles of A	1	1	47
	RL A	Rotate A left	1	1	E7
	RLC A	Rotate A left through carry	1	1	F7
	RR A	Rotate A right	1	1	77
	RRC A	Rotate A right through carry	1	1	67
Input/Output	IN A, P_p	Input port to A	1	2	08,09,0A
	OUT P_pA	Output A to port	1	2	90,39,3A
	MOVD A,P_p	Input expander port to A	1	2	0C-0F
	MOVD P_p,A	Output A to expander port	1	2	3C-3F
	ANLD P_p,A	And A to expander port	1	2	9C-9F
	ORLD P_p,A	Or A to expander port	1	2	8C-8F
Registers	INC R_r	Increment register	1	1	18-1F
	INC @R	Increment data memory	1	1	10-11
Branch	JMP addr	Jump unconditional	2	2	04,24,33,64, 84,A4,C4,E4
	JMPP @A	Jump indirect	1	2	B3
	DJNZ R,addr	Decrement register and jump on R not zero	2	2	E8-EF
	JC addr	Jump on carry = 1	2	2	F6
	JNC addr	Jump on carry = 0	2	2	E6
	JZ addr	Jump on A zero	2	2	C6
	JNZ addr	Jump on A not zero	2	2	96
	JT0	Jump on T0 = 1	2	2	36
	JNT0	Jump on T0 = 0	2	2	26
	JT1 addr	Jump on T1 = 1	2	2	56
	JNT1 addr	Jump on T1 = 0	2	2	46
	JTF addr	Jump on timer flag	2	2	16
Subroutine	CALL	Jump to subroutine	1	2	14,34,54,74, 94,B4,D4,F4
	RET	Return	1	2	83
Flags	CLR C	Clear carry	1	1k	97
	CPL C	Complement carry	1	1	A7
Data Moves	MOV A,R_r	Move register to A	1	1	F8-FF
	MOV A,@R	Move data memory to A	1	1	F0-F1
	MOV A,#data	Move immediate to A	2	2	23
	MOV R_r,A	Move A to register	1	1	A8-AF
	MOV @R,A	Move A to data memory	1	1	A0-A1
	MOV R_r,#data	Move immediate to register	2	2	B8-BF
	MOV @R,#data	Move immediate to data memory	2	2	B0-B1
	XCH A,R_r	Exchange A and register	1	1	28-2F
	XCH A,@R	Exchange A and data memory	1	1	20-21
	XCHD A,@R	Exchange nibble of A and register	1	1	30-'31
	MOVP A,@A	Move to A from current page	1	2	A3
Timer/Counter	MOV A,T	Read timer/counter	1	1	42
	MOV T,A	Load timer/counter	1	1	62
	STRT T	Start timer	1	1	55
	STRT CNT	Start counter	1	1	45
	STOP TCNT	Stop timer/counter	1	1	65
A/D Converter	RAD	Move conversion result register to A	1	2	80
	SEL AN0	Select analog input zero	1	1	85
	SEL AN1	Select analog input one	1	1	95
Interrupts	EN I	Enable external interrupt	1	1	05
	DIS I	Disable external interrupt	1	1	15
	EN TCNTI	Enable timer/counter interrupt	1	1	2 5
	DIS TCNTI	Disable timer/counter interrupt	1	1	35
	RET I	Return from interrupt	1	2	93
	NOP	No operation	1	1	00

SYMBOLS AND ABBREVIATIONS USED

A	Accumulator
addr	11-Bit Program Memory Address
AN0, AN1	Analog Input 0, Analog Input 1
CNT	Event Counter
data	8-Bit Number or Expression
I	Interrupt
P	Mnemonic for "in-page" Operation
P_p	Port Designator (P = 1, 2 or 4-7)
R_r	Register Designator (r = 0–7)
T	Timer
T0, T1	Test 0, Test 1
#	Immediate Data Prefix
@	Indirect Address Prefix

FUNCTIONAL DESCRIPTION

PROGRAM MEMORY

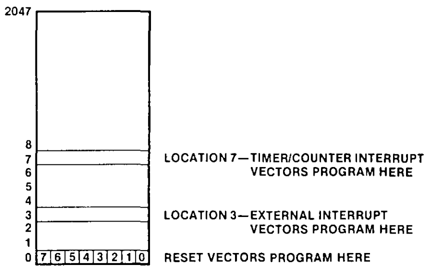
The 8022 program memory consists of 2048 words 8 bits wide which are addressed by the program counter. The memory is ROM which is mask programmable at the factory. No external ROM expansion capability is provided. There are three locations in program memory of special importance.

Location 0: Activating the RESET line of the processor causes the first instruction to be fetched from location 0.

Location 3: Activating the interrupt input line of the processor (if interrupt is enabled) causes a jump to subroutine.

Location 7: A timer/event counter interrupt resulting from a timer/counter overflow causes a jump to subroutine (if timer/counter interrupt is enabled).

Therefore, the first instruction to be executed after initialization is stored in location 0, the first word of an external interrupt service routine is stored in location 3, and the first word of a timer/event counter interrupt service routine is stored in location 7.



PROGRAM MEMORY MAP

Program memory can be used to store constants as well as program instructions. The MOVP instruction allows easy table lookup for constants and display formatting.

DATA MEMORY

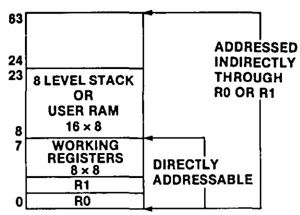
On-chip data memory is organized as 64 words eight bits wide. All locations are indirectly addressable and eight designated locations are directly addressable. Also included in the data memory is the program counter stack, addressed by a 3-bit stack pointer.

The first eight locations (0-7) of the array are designated as working registers and are directly addressable by any of the 11 direct register instructions. These locations are readily accessible for a variety of operations with a minimum number of instruction bytes required for their manipulation. Thus, they are usually used to store frequently accessed intermediate results. The DJNZ instruction makes very efficient use of the working registers as program loop counters by allowing the programmer to decrement and test the register in a single instruction.

Registers 0 and 1 have yet another function in that they can be used to indirectly address all locations in the data memory using the indirect register instructions. These two RAM pointer registers are especially useful for repetitive type operations on adjacent memory locations. The indirect register instruction specifies which pointer register to use and the content of the pointer register is used to address a location in RAM. The contents of the addressed location are used during the execution of the instruction and may be modified. The pointer registers may also point to registers 0-7, if desired.

Locations 8-23 serve a dual role in that they contain the 8-level program counter stack, two RAM locations per level. The program counter stack enables the processor to keep track of the return addresses generated by interrupts or CALL instructions by storing the contents of the program counter prior to servicing the subroutine. A 3-bit stack pointer determines which of the program counter stack's eight register pairs will be loaded with the next return address generated. The stack pointer, when initialized to 000 by RESET, points to RAM locations 8 and 9. The first subroutine jump or interrupt results in the program counter contents being transferred to locations 8 and 9. The stack pointer is then incremented by one and points to locations 10 and 11 in anticipation of another CALL. The end of a subroutine, which is signaled by a return instruction (RET or RETI), causes the stack pointer to be decremented and the contents of the resulting register pair to be transferred to the program counter.

Since the program counter's addresses are 11 bits long, two bytes or registers must be used to store a single address. Thus, the 16-byte program counter stack permits up to a total of 8 levels of subroutine nesting without overflowing the stack. If overflow does occur, the deepest address stored (locations 8 and 9) will be overwritten and lost since the stack pointer overflows from 111 to 000. It also underflows from 000 to 111. If a particular application does not require 8 levels of nesting, tthe unused portion of the program counter stack may be used as any other indirectly addressable RAM location. For example, if only 3 levels of subroutine nesting are used, then only locations 8-13 need be reserved for the program counter stack, and locations 14-23 can be used for data storage.



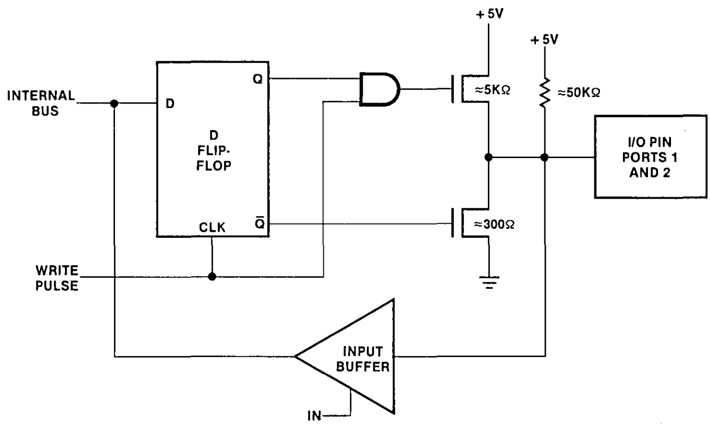
DATA MEMORY MAP

INPUT/OUTPUT

The 8022 has 26 lines which can be used for digital input or output functions. These lines are organized as 3 ports of 8 lines, each of which serve as either inputs, outputs, or bidirectional ports, and 2 test inputs which can alter program sequences when tested by conditional jump instructions.

Ports 1 and 2 have identical operating characteristics and are both quasi-bidirectional. That is, each line may serve as an input, an output, or both. Data written to these ports is statically latched and remains unchanged until rewritten. As inputs, these lines are non-latching; i.e., inputs must be present until read by an input instruction. Inputs are fully TTL compatible and all outputs will drive at least one standard TTL load. Two lines of port 1 (P10 and P11) are designated as high current drive lines and have the ability to sink 7 mA. In addition, these pins may be paralleled for 14 mA output if the output logic states are always the same. The high current output lines eliminate the need for discrete transistors in many applications.

The lines of ports 1 and 2 are quasi-bidirectional because of their output structure which allows them to be used as inputs, outputs, or both, even though as outputs they are statically latched.

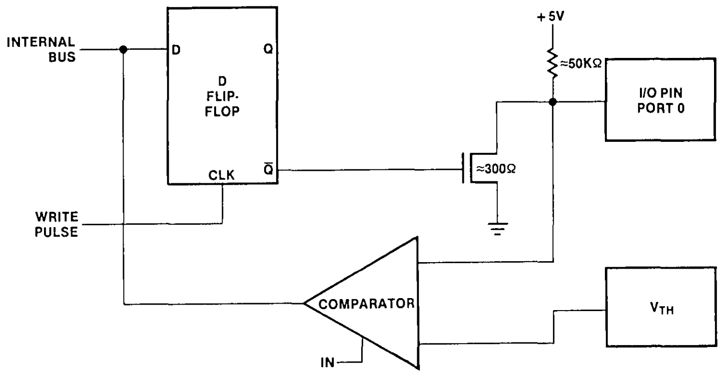


QUASI-BIDIRECTIONAL PORT STRUCTURE

Each line is continuously pulled up to +5V through a relatively high impedance device (~50 kΩ). This pullup is sufficient to provide the source current for a TTL high level, yet can be pulled low by a standard TTL gate, thus allowing the same pin to be used both as an input and output. When writing a "0" or low value to these ports, a low impedance device (~300Ω) overcomes the high pullup and provides TTL current sinking capability. When writing a "1", a large current is momentarily supplied through a relatively low impedance device (~5kΩ) to allow a fast data transfer. After a short time (less than one instruction cycle) the low impedance device is shut off and the small pullup maintains the "1" level indefinitely. In this situation, an input device capable of overriding the small amount of sustaining current supplied by the pullup device can be read. (Alternatively, the data written cn be read.) So, by writing a "1" to any particular pin that pin can serve either as a true high-level latched output pin, or as just a pullup resistor on an input. This allows maximum user flexibility in selecting his input or latched output lines, with a minimum of external components.

PORT 0 COMPARATOR INPUTS

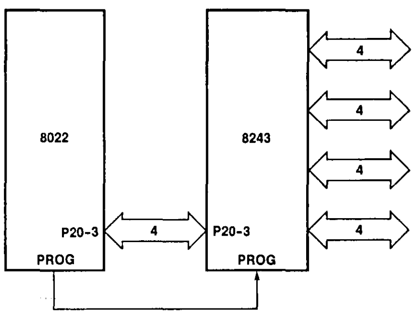
Port 0 has been modified from the standard quasi-bidirectional structure to allow an optional open drain configuration with comparator inputs. The low impedance pullup device has been eliminated and the high impedance pullup is optional. Thus, the user can choose via a mask programmable selection each line of port 0 to be either quasi-bidirectional with a high impedance or true open-drain. The open drain configuration allows the line to sink current through the low impedance pulldown device or to float in the high output state. More importantly, the open drain configuration makes port 0 very easy to drive when it is used as inputs. The input circuitry for each line of port 0 includes a voltage comparator which amplifies the voltage difference between the input port line and the port 0 threshold reference pin (V_{TH}). The voltage gain of the comparator is sufficient to sense a 100 mV input differential withn the range V_{SS} to $V_{CC}/2$.



PORT 0 I/O STRUCTURE

If V_{TH} is allowed to float, it will bias itself to the digital switch point of the other ports, and port 0 behaves as a set of normal digital inputs. However, by biasing V_{TH}, the switch point can be both tightly controlled and adjusted. Common uses for this would include high noise margin inputs ($V_{CC}/2$), unusual logic level inputs as from a diode isolated keyboard, analog channel expansion, and direct capacitive touchpanel interface. The comparator action is automatic and the port is read just as any other port.

In addition to the 26 digital I/O lines contained on-board the 8022, a user can obtain additional I/O lines by utilizing the Intel® 8243 I/O expander chip or standard TTL. The 8243 interfaces to 4 port lines of the 8022 (lower half of port 2) and is strobed by the PROG line of the 8022.



I/O EXPANDER INTERFACE

The 8243 contains four 4-bit I/O ports which serve as extensions of the on-chip I/O and are addressed as ports 4-7. The following operations may be performed on these ports:

1. Transfer Accumulator to Port
2. Transfer Port to Accumulator
3. And Accumulator to Port
4. Or Accumulator to Port

A 4-bit transfer from a port to the lower half of the accumulator sets the most significant four bits to zero. Each transfer consists of two 4-bit nibbles. The first contains the "opcodes" and port address, and the second contains the actual 4 bits of data. A high-to-low transition of the PROG line indicates that address is present while a low-to-high transition indicates the presence of data.

TEST AND INTERRUPT INPUTS

In addition to the 24 general purpose I/O lines which comprise ports 0, 1, and 2, the 8022 has two inputs which are testable via conditional jump instructions, T0 and T1. These pins allow inputs to cause program branches without the necessity to load an input port into the accumulator. T0 and T1 have other functions as well.

The Test 0 pin serves as an external interrupt input as well as a testable input. An interrupt sequence is initiated by applying a low "0" level input to the T0 pin when external interrupt is enabled. Interrupt is level triggered and active low to allow "WIRE ORING" of several interrupt sources at the input pin. When an interrupt is detected, it causes a "jump to subroutine" at location 3 in program memory as soon as all other cycles of the current instruction are complete. At this time, the program counter contents are saved in the program counter stack, but the remaining status of the processor is not. Unlike the 8048, the 8022 does not contain a program status word. Thus, when appropriate, the carry and auxiliary carry flags are saved in software, as the accumulator is. The routine shown below saves the accumulator and the carry flags in only four bytes.

Instructions	Bytes	Comments
MOV R6,A	1	;save accumulator
CLR A	1	;clear accumulator
DA A	1	;convert carry flags into sixes
MOV R7,A	1	;save status of carry flags

The end of an interrupt service subroutine is marked by the execution of a Return from Interrupt instruction (RETI). Prior to returning from the interrupt subroutine

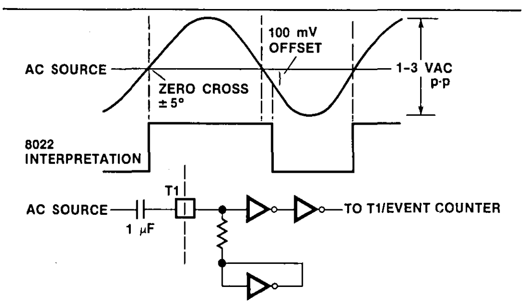
however, the status of the accumulator and the carry flags are restored in software. The following routine restores the status of the accumulator and the carry flags, which was previously saved, in five bytes.

Instructions	Bytes	Comments
MOV A,R7	1	;restore carry flags status to
Add A,#0AAH	2	;accumulator and set/clear carry flags
MOV A,R6	1	;restore accumulator
RETI	1	;return

The interrupt system is single level in that once an interrupt is detected, all further interrupt requests are ignored until execution of a RETI re-enables the interrupt input logic. This sequence holds true also for an internal interrupt generated by timer overflow. If an external interrupt and an internal timer/counter generated interrupt are detected at the same time, the external source will be recognized. If needed, a second external interrupt can be created by enabling the timer/counter interrupt, loading FFH in the counter (one less than terminal count) and enabling the event counter mode. A low-to-high transition on the T1 input will then cause an interrupt vector to location 7.

The Test 1 pin, in addition to being a testable input, serves two other important functions. It can be used as an input pin to the external event counter, as previously mentioned, and it can be used to detect the zero crossing point of slow moving AC signals. Execution of the STRT CNT instruction puts the T1 pin in the counter input mode by connecting T1 to the counter and enabling the counter. Subsequent low-to-high transitions on T1 will cause the counter to increment. Note that this operation differs from the rest of the MCS-48 devices, which increment the counter on high-to-low transitions. This change was made on the 8022 to take advantage of the accuracy of the rising edge detection on the zero cross circuitry. The maximum rate at which the counter may be incremented is once per three instruction cycles (every 30 μs when using a 3 MHz crystal) — there is no minimum frequency.

In addition to serving as a testable input and as the counter input, the T1 pin has special circuitry to detect when an AC signal crosses its average DC level. When driven directly, this pin responds as a normal digital input. To utilize the zero cross detection mode, an AC signal of approximately 1-3 VAC p-p magnitude and a maximum frequency of 1 kHz is coupled through an external capacitor (1 μF) to the T1 pin.



ZERO-CROSS DETECTION

The internal digital state is sensed as a zero until the rising edge crosses the DC average level, when it becomes a one. This is accomplished by the self-biasing high gain amplifier which is included in the T1 input. This circuit biases the T1 input exactly at its switching point, such that a small change will cause a digital transition to occur. This digital transition takes place within 5 degrees of the zero point. The digital value of T1 remains a one until the falling edge of the AC input drops approximately 100 mV below the switching point of the rising edge (100 mV below the zero point, if the digital transition occurred exactly at the zero point). The 100 mV offset is created by hysterisis and eliminates chattering of the internal signal caused by the external noise.

The zero cross detection capability allows the user to make the 60 Hz power signal the basis for this system timing. All timing routines, including time-of-day, can be implemented using the zero cross detection capability of T1 and its conditional jump instructions. In addition, the zero cross detection feature can be used in conjunction with the timer interrupt to interrupt processing at the zero voltage point. This enables the user to control voltage phase sensitive devices such as triacs and SCRs, and to use the 8022 in applications such as shaft speed and angle measurement.

ANALOG TO DIGITAL CONVERTER

The 8022 contains on-chip a complete hardware implementation of an 8-bit analog to digital (A/D) converter with two multiplexed analog inputs. The A/D converter utilizes a successive approximation technique to provide an updated conversion once every four instruction cycles (i.e., once every 40 μs) with a minimum of required software.

The A/D converter consists of four main parts, the input circuitry, a series string of resistors, a voltage comparator, and the successive approximation logic. The two analog inputs are multiplexed on-chip and selected via software by the SEL AN0 and SEL AN1 instructions. Besides selecting one of the analog inputs, these instructions restart the conversion sequence which operates continuously. Restarting a conversion sequence deletes the conversion in progress but does not effect the result of the previous conversion which is stored in the conversion result register. The continuous operation of the A/D converter saves program space and time by allowing the user obtain multiple readings from a given input with only one select instruction. To obtain a valid conversion reading, the user must provide the analog input signal no later than the beginning of the select instruction cycle. The analog input is then sampled by the A/D converter and maintained internally. This voltage becomes one input to the voltage comparator which amplifies the difference between the analog input and the voltage tap on the series resistor string.

The series resistor string is connected between the A/D reference pin (V_{AREF}) and ground (AV_{SS}). It is comprised of 256 identical resistors which divide the voltage between these two pins into 256 identical voltage steps. This configuration gives the converter its inherent monotonicity. The range of V_{AREF} in which full 8-bit resolution can be provided is between $V_{CC}/2$ and V_{CC}.

Thus, the user is given a minimum voltage range from ground to $V_{CC}/2$ and a maximum range from ground to V_{CC} over which 8-bit resolution is insured.

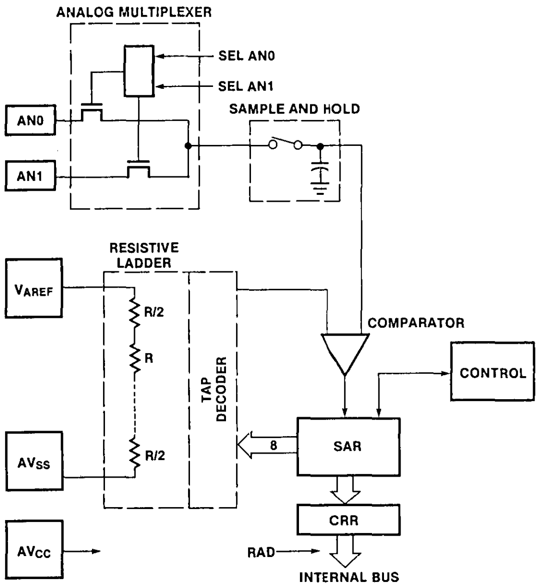
The voltage tap on the series resistor string is selected by the resistor ladder decoder. This decoder is driven by the 8-bit successive approximation register (SAR). Each bit of the SAR is set in succession MSB to LSB and a voltage comparison between the selected resistor ladder voltage and the analog input voltage is performed after the setting of each bit. The result of each comparison determines whether the particular bit will remain set or be reset. All comparisons are performed automatically by the on-chip A/D hardware. At the end of 8 comparisons the SAR contains a valid digital result which is then latched into the conversion result register (CRR). The RAD instruction (read A/D) loads the conversion result from the CRR to the accumulator of the 8022.

As mentioned previously, the software and time required to perform an A/D conversion is optimized by the 8022's on-chip A/D converter configuration. Typical software for reading two sequential A/D conversions and storing them in data memory is shown below:

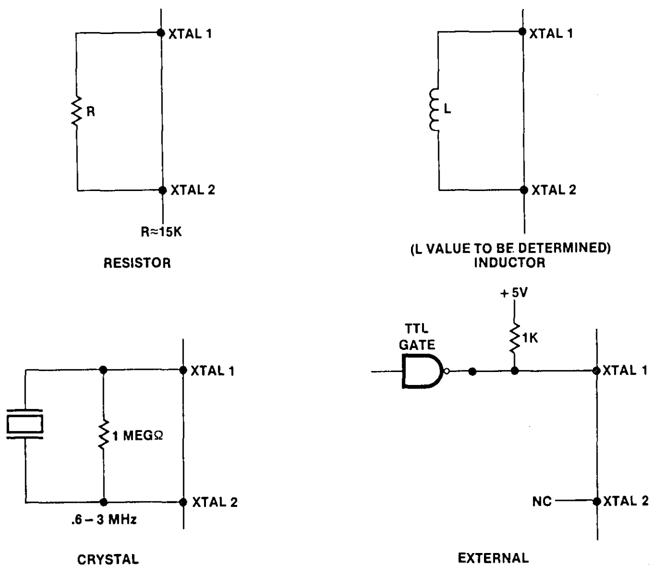
First Conversion 50 µs 4 bytes	SEL AN0	;Starts conversion of AN0 input
	MOV R0,#24	;Set up memory pointer
	RAD	;First conversion value to accumulator
Second Conversion 40 µs 3 bytes	MOV @R0,A	;Store first conversion value
	INC R0	;Increment memory location
	RAD	;Second conversion value to accumulator

Note that the second conversion occurs without a second select instruction being used. Rather, the continuous operation of the A/D converter provides an updated digital value 4 instruction cycles after the first.

To insure maximum accuracy from the A/D converter, separate power supply pins (AV_{CC} and AV_{SS}) and a substrate pin (SUBST) have been provided. Supplying the power supply pins with a well filtered and regulated voltage supply minimizes the effect of power supply variance and system noise. The substrate pin should be bypassed to ground through a 500 pF to 0.001 µF capacitor.



A/D CONVERTER BLOCK DIAGRAM



FREQUENCY REFERENCE OPTIONS

OSCILLATOR AND CLOCK

The 8022 contains its own on-board oscillator and clock circuit, requiring only an external timing control element. This control element can be a crystal, inductor, resistor, or clock in. The capacitor normally required in resistor or inductor timing control operation is integrated onto the 8022. All internal time slots are derived from the external element, and all outputs are a function of the oscillator frequency. Pins X1 and X2 are used to input the particular control element. An instruction cycle consists of 10 states, and each state is a time slot of 3 oscillator periods. Therefore, to obtain a 10 μs instruction cycle, a 3 MHz crystal should be used.

TIMER/COUNTER

An interval timer/counter is available to enable the user to keep track time elapsed or number of events occurred, during normal program execution and flow.

By a MOV T,A instruction, the contents of the accumulator are loaded to the timer. At the STRT T command an internal prescaler is zeroed and thereafter increments once each 30 input clocks (once each single cycle instruction, twice each double cycle instruction). The prescaler is a divided by 32. At the (11111) to (00000) transition the timer is incremented. The timer is 8 bits and an overflow (FFH) to (00H) timer flag is set along with the timer interrupt, if enabled. A conditional branch instruction (JTF) is available for testing this flag, the flag being reset each test. This instruction must also be used to initialize the timer overflow flag after a RESET instruction, as RESET does not perform this function. Total count capacity for the timer is $2^8 \times 2^5 \doteq 8192$ or 81.9 ms at a 10 μs cycle time. Contents of the timer are moved to the accumulator by the MOV A,T instruction without disturbing the counting process.

The timer may also be used as an event counter. After a STRT CNT command, the 8022 will respond to a low-to-high transition on the Test 1 pin by incrementing the timer. Transitions can occur no faster than once each three instruction cycles.

The timer and event functions are exclusive. Counting or timing may be started or stopped (STOP TCNT) at will.

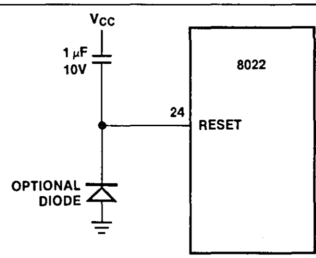
CPU

The 8022 CPU has arithmetic and logical capability. A wide variety of arithmetic and logic instructions may be exercised, which affect the contents of the accumulator, and/or direct or indirect scratchpad locations. Provisions have been made for simplified BCD arithmetic capability through the use of the DAA, SWAP A, and XCHD instructions. In addition, MOVP A,@A allows table lookup for display formatting and constants. Jump conditions such as zero, not zero refer to the accumulator contents at the time of the condition.

RESET

The 8022 may be used in systems with poorly regulated and noisy power supplies. A useful feature is to sense when the power supply dips and quickly recovers, and do a reset to prevent continued operation with incorrect data. This feature may be implemented on the 8022 by connecting a diode between the RESET node and ground.

Including the diode in the reset circuitry forces a reset to occur if the power supply experiences a very sudden voltage glitch. Specifically, if the power supply drops approximately 1.5V and recovers after at least a few nanoseconds, a reset will occur. Without the diode, a power supply interruption of less than 1 ms will not cause a power-on reset.



POWER ON RESET